1. Description

These N-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

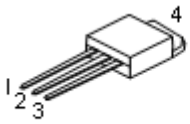
2. Features

- $R_{DS(ON)}$=72 mΩ@V_{GS}=10V
- Improved dv/dt capability
- Fast switching
- 100% EAS guaranteed
- Green device available

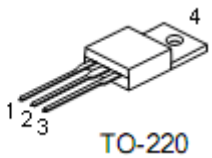
3. Applications

- Networking
- Load switch
- Led applications

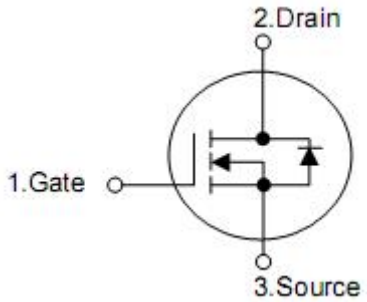
4.Symbol



TO-251



TO-220



Pin	Function
1	Gate
2	Drain
3	Source
4	Drain

5. Absolute maximum ratings

(T_A=25°C,unless otherwise noted)

Parameter		Symbol	Rating	Units
Drain-source voltage		V_{DSS}	100	V
Gate-source voltage		V_{GSS}	±20	V
Operating junction temperature range		T_J	-50 to 150	ºC
Storage temperature range		T_{STG}	-50 to 150	ºC
Continuous drain current	T_C=25ºC	I_D	15	A
	T_C=100ºC		9.5	A
Pulsed drain current[1]		I_{DM}	60	A
Maximum power dissipation	T_C=25 ºC	P_D	50	W
	Derate above 25 ºC		0.4	W/ ºC

6. Thermal characteristics

Parameter	Symbol	Rating	Unit
Thermal resistance,Junction-ambient	$R_{\theta JA}$	62	ºC/W
Thermal resistance,Junction-case	$R_{\theta JC}$	2.5	ºC/W

7. Electrical characteristics

(T_A=25°C,unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Drain-source breakdown voltage	BV_{DSS}	V_{GS}=0V,I_D=250uA	100	-	-	V
BV_{DSS} temperature coefficient	$\triangle BV_{DSS}/\triangle T_J$	Reference to 25°C, I_D=1mA	-	0.05	-	V/°C
Zero gate voltage drain current	I_{DSS}	V_{DS}=100V, V_{GS}=0V T_J=25°C	-	-	1	μA
		V_{DS}=80V, V_{GS}=0V T_J=125°C	-	-	10	
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μA	1.2	1.6	2.5	V
$V_{GS(th)}$ temperature coefficient	$\triangle V_{GS(th)}$		-	-5	-	mV/°C
Forward transconductance	gfs	V_{DS}=10V,I_D=3A	-	8.7	-	S
Gate leakage current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=10V,I_{DS}=5A	-	72	90	mΩ
Gate resistance	R_g	V_{DS}=0V, V_{GS}=0V,f=1MHz	-	1.3	2.6	Ω
Diode forward voltage	V_{SD}	I_{SD}=1A, V_{GS}=0V, T_J=25°C	-	-	1	V
Reverse recovery time[2]	t_{rr}	I_S=1A ,V_{GS}=30V dI_{SD}/dt=100A/μs, T_J=25°C	-	-	-	nS
Reverse recovery charge[2]	Q_{rr}		-	-	-	nC
Input capacitance	C_{iss}	V_{DS}=50V,V_{GS}=0V, f=1MHz	-	1480	2150	pF
Output capacitance	C_{oss}		-	480	700	
Reverse transfer capacitance	C_{rss}		-	35	55	
Turn-on delay time[2.3]	$t_{d(on)}$	V_{DD}=30V,I_D=1A, R_G=3.3Ω,V_{GS}=10V	-	2.9	6	ns
Rise time[2.3]	t_r		-	9.5	18	
Turn-off delay time[2.3]	$t_{d(off)}$		-	18.4	35	
Fall time[2.3]	t_f		-	5.3	10	
Total gate charge[2.3]	Q_g	V_{DS}=48V,V_{GS}=10V I_D=5A	-	9.3	13	nC
Gate-source charge[2.3]	Q_{gs}		-	2.1	4.2	
Gate-drain charge[2.3]	Q_{gd}		-	1.8	4	
Continuous source current	I_S	V_G=V_D=0V, force current	-	-	15	A
Pulsed source current	I_{SM}		-	-	60	A

Note : 1. Repetitive rating, pulse width limited by maximum junction temperature

2. The data tested by pulse, pulse width≤300us duty cycle≤2%.

3. Essentially independent of operating temperature.

8. Test circuits and waveforms

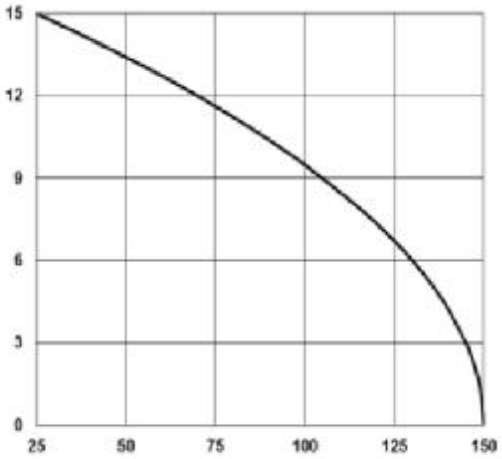


Fig.1 Continuous Drain Current vs.TC

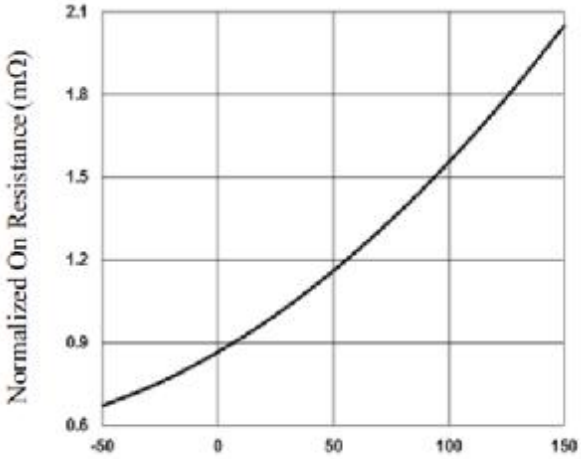


Fig.2 Normalized RDSON vs.TJ

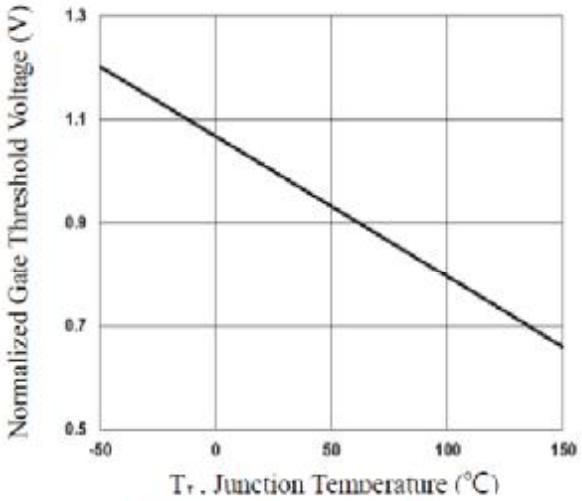


Fig.3 Normalized Vth vs. TJ

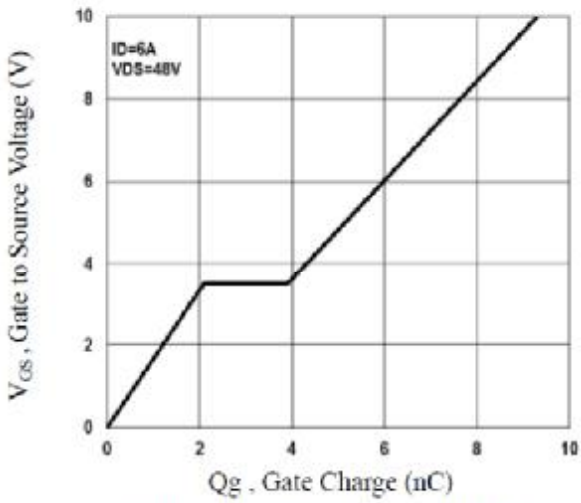


Fig.4 Gate Charge Characteristics

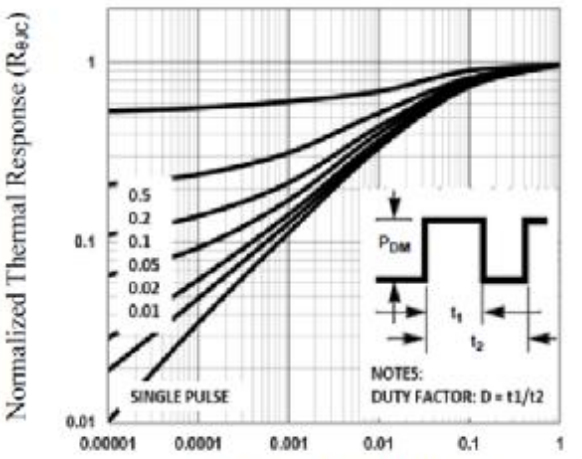


Fig.5 Normalized Transient Impedance

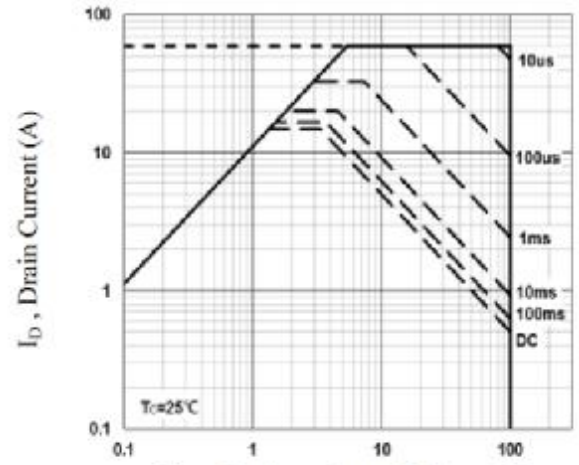


Fig.6 Maximum Safe Operation Area

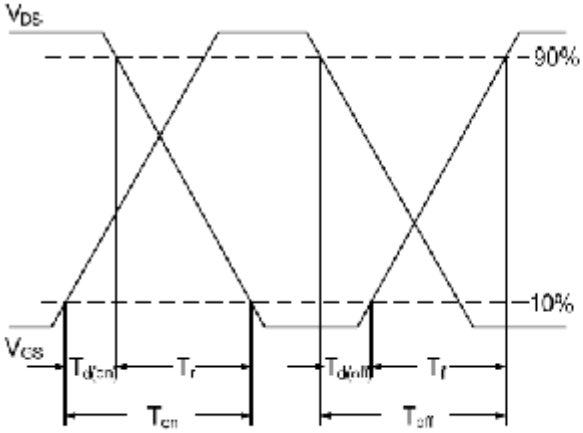


Fig.7 Switching Time Waveform

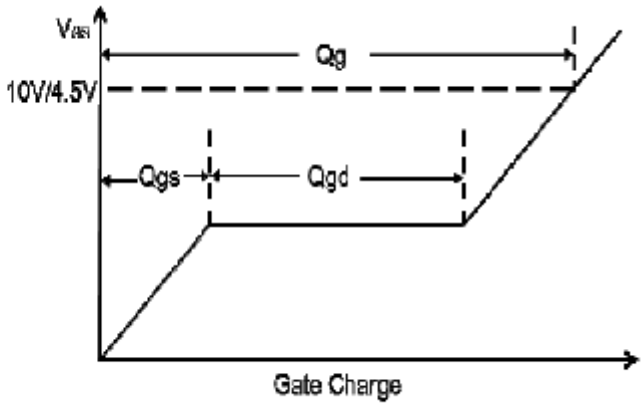


Fig.8 Gate Charge Waveform